Simulation Study of the Three-Level Boost DC-DC Converter with Full ZVS for PV Application

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***Abstract*— This paper presents the full zero voltage switching three-level boost dc-dc converter. The boundary conduction mode and snubber capacitors provide zero voltage switching operation in the whole range of operation. Analytical estimation and simulation results have proved the proposed idea. In advance, it was demonstrated that the multi-cell structure along with an interleaved control technique provide high efficiency performance and continuous input current that makes it a promising solution for photovoltaic applications.**

***Index Terms*-- dc-dc converters, control of multilevel converters, multilevel converters, zero voltage switching.**

I. INTRODUCTION

In recent years, renewable energy has attracted increasing attention. Renewable energy interface converters are required to inject renewable energy into the power distribution grid. In particular, solar inverters have become extremely popular on the modern power electronics market. At the same time, traditionally, passive magnetic components required for boost capabilities and output filtering are the most expensive components. As a result, the researchers concentrate efforts on the reduction of the passive components. Good state of the art of the existing topologies is reported in [1]. It is obvious that the solutions discussed are suitable for industrial applications in terms of cost and reliability. Some studies [2]-[5] propose novel ideas that provide a wide range of regulation capability but have quite a complex structure.

Novel trends in power electronics show that future is connected with high switching frequency semiconductors and wide band-gap semiconductors in particular [6], [7]. High switching frequency semiconductors are a key issue in the high power density devices. The challenge is still in their cost.

Soft-switching techniques provide an important direction in power electronics as well. These techniques allow reduction of the losses in semiconductors and as a result, the switching frequency can be raised or the heat sink may shrink in size.

Along with soft-switching techniques and proper packaging design, extremely fast switching power electronics devices are achievable. There are several 600 V Si MOSFET families with fast body diode suitable for inverter applications.

Today modular and multi-cell structures are extremely popular due to the introduction of novel semiconductors, particularly in high voltage high power applications [8]-[15]. At the same time, modular and interleaved topologies can satisfy extremely high efficiency demand and shrink the heat sink in the power electronics converters.

The aim of the paper is to demonstrate the full soft-switching approach for the Three-Level Multi-Cell (3L MC) [13] boost dc-dc converter with continuous input current, which is an interface converter for Photovoltaic (PV) applications.

A PV system of 18 serial panels is a voltage source for the proposed solution. Fig. 1 shows the resulting input PV curve. It is well known that solar panels provide limited voltage and current that follows an exponential I-V curve. Table 1 presents the main specifications of one of the commercial solar module (LDK 185D-24(s)) [16].

Several working points are indicated in Fig. 1. Even low but equally distributed solar irradiation does not require extremely high boost (point 2). The high boost capability is demanded in the partly shadowed mode where only some of the panels in the array have lower irradiation (point 3). It can be seen that the Maximum Power Point (MPP) with maximum irradiation corresponds to the voltage source inverter (VSI) mode that does not require the voltage boost feature (point 1).

Fig. 2 illustrates the proposed full soft-switching solution with continuous input current based on the 3L boost dc-dc converter.

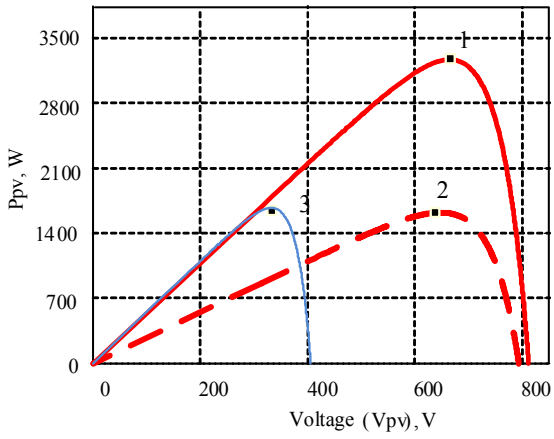

Fig. 1. Case study PV curve.

TABLE I.
MAIN PARAMETERS FROM THE DATASHEET OF THE REAL PANELS.

Characteristic	Unit	Value
Nominal output power (Pmax)	W	185
Voltage at Pmax	V	36.9
Current at Pmax	A	5.02
Open circuit voltage (Voc)	V	45.1
Short circuit current (Isc)	A	5.48

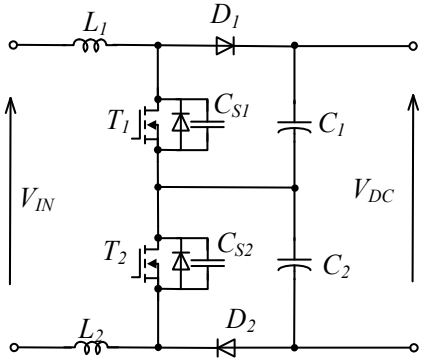

Fig. 2. 3L boost dc-dc converter.

II. OPERATION PRINCIPLE OF THE PROPOSED SOLUTION

Fig. 3 illustrates the operation diagrams of the single boost cell. The main idea lies in using the Boundary Conduction Mode (BCM) of the inductor current. Along with snubber capacitors C_S, full Zero Voltage Switching (ZVS) operation is achievable.

3L topology has two possible boost states. In the first case when both transistors are conducting, full input voltage is applied to the inductors, as a result higher boost factor B_2 is expected:

$$B_2 = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - D_{S2}}, \quad (1)$$

where D_{S2} is the conduction duty cycle of both transistors.

In the second case (only one transistor is conducting), a decreased value (V_{IN}-$V_{DC}/2$) is applied to the inductors. The boost factor B_1 is expressed as:

$$B_1 = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - \frac{D_{S1}}{2}}, \quad (2)$$

where D_{S1} is the conduction duty cycle of a single transistor.

Such solution has flexible boost regulation and more freedom in the BCM control. At combined regulation, the boost factor B can be expressed as:

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - \frac{D_{S1}}{2} - D_{S2}}. \quad (3)$$

Fig 4 illustrates also the operation principle by means of equivalent circuits. Switching signals of the transistors T_1 and T_2 show that both boost states are applicable in such approach. During the time interval t_0-t_1 (Fig. 4*a*), both transistors are conducting and inductor current is raised. At the moment t_1, transistor T_2 is turned off under ZVS due to the snubber capacitor (Fig. 4*b*). During the time interval t_1-t_2, only transistor T_1 is conducting and inductor current continues rising through the capacitor C_2 and the diode D_2. At the moment t_2, transistor T_1 is turned off under ZVS also due to the snubber capacitor (Fig. 4*c*). After that inductor current falls through the capacitors C_1, C_2 and the diodes D_1, D_2.

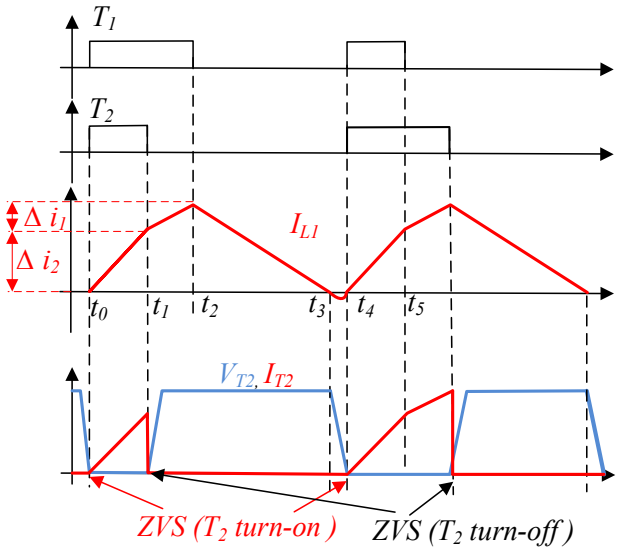

Fig. 3. Operation diagrams of the 3L boost dc-dc converter.

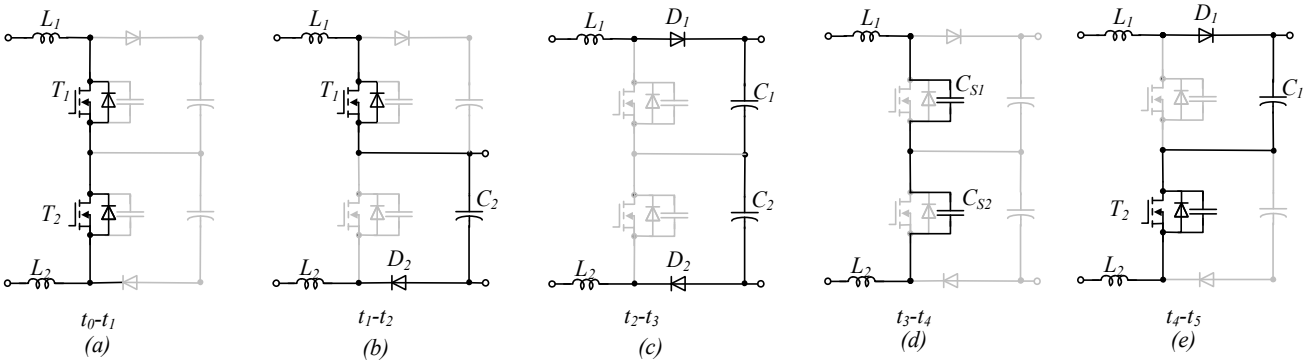

Fig. 4. Equivalent circuits of the 3L boost dc-dc converter.

After reaching zero inductor current, the resonance phenomenon occurs. As a result, during the time interval t_3-t_4, inductor current has an opposite direction and snubber capacitors are discharging (Fig. 4*d*).

At the moment t_4, snubber capacitor voltage is around zero. At this moment transistor T_2 is turned on under ZVS (Fig. 4*e*).

A similar process continues during the next time intervals. Due to the resonance phenomenon, diodes are under soft switching operation as well.

III. Component Design Guidelines

This section describes the component selection guidelines. The main aim is to estimate inductors and snubber capacitors in order to provide ZVS in the full working range that corresponds to the PV curve. In particular, the BCM must be provided for double range of the input voltage.

Let us define the condition of the BCM for a general case.

$$\frac{\Delta i_1 + \Delta i_2}{2} = I_{IN}, \tag{4}$$

where $\Delta i_1+\Delta i_2$ is a total current ripple, I_{IN} is average input current (Fig. 3).

Taking into account equivalent circuits (Fig. 4) for each time interval it is possible to express the ripple components as:

$$\Delta i_2 = \frac{V_{IN}}{L} \cdot T \cdot D_{S2}, \tag{5}$$

$$\Delta i_1 = \frac{V_{IN} - \frac{V_{DC}}{2}}{L} \cdot T \cdot D_{S1}, \tag{6}$$

where $L=L_1+L_2$ is a total inductance, T is a time duty of the switching cycle (Fig. 3).

After introducing Eqs. (5) and (6) into Eq. (4), the following expression is derived:

$$V_{DC} = 2 \cdot V_{IN} \frac{D_{S1} + D_{S2}}{D_{S1}} - 4 \cdot \frac{L \cdot I_{IN}}{T \cdot D_{S1}}. \tag{7}$$

This equation shows how the dc-link voltage depends on the input voltage V_{IN}, the input current I_{IN} and the control signals under the BCM condition.

Fig. 5 shows two three-dimensioning surfaces. The first surface links the variables D_{S1}, D_{S2} and V_{IN} under the constant I_{IN} , L and T. and the BCM condition and corresponds to Eq. (7). The second surface links the same variables and corresponds to Eq. (3). As a result, changing the inductance value L, it is possible to derive several curves that correspond to the crossing surfaces of Eqs. (7) and (3).

Fig. 6 illustrates a family of projections of the curves with different inductances. It can be seen that in order to achieve the BCM, a certain inductance value must be selected. At the same time, taking into account that $D_{S1}+D_{S2}\leq 1$ it can be seen that the range of the input voltage variation under the BCM condition is limited. It means that in some working points the BCM is not achievable, but the Discontinuous Conduction Mode (DCM) can be used as well. The drawback of the DCM lies in a more complex dynamic behavior of the closed loop control system.

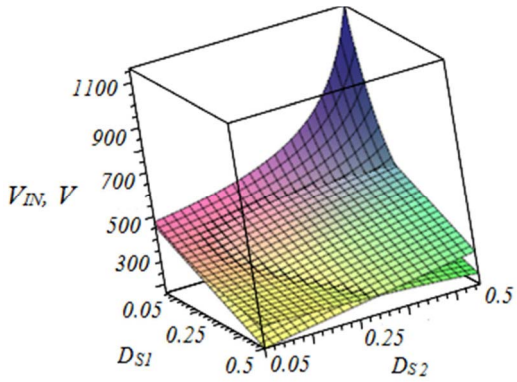

Fig. 5. Two three-dimensioning surfaces that link variables D_{S1}, D_{S2} and V_{IN} under the BCM condition, $L=.100\ \mu H$.

Finally, the total inductance $76\ \mu H$ was selected. This value can provide full ZVS operation and the BCM in most of the operation points.

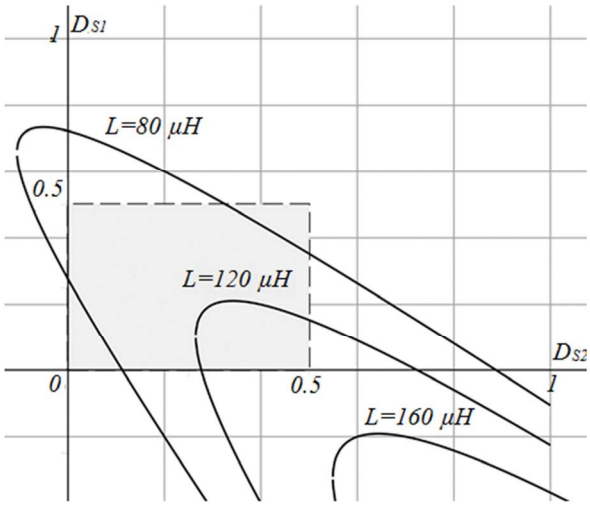

Fig. 6. Operation range under the BCM condition with different inductances.

IV. Simulation Study of the ZVS Operation

To verify the idea described above, a PSIM simulation model was realized. Table II shows the parameters used for the simulation.

TABLE II.
System Parameters Used for Simulations

Parameter	*Value*
Input voltage range	*325 V…800 V*
Output dc voltage	*650 V*
Maximum power per cell	*1800 W*
L_1, L_2	*38 μH*
C_{S1}, C_{S2}	*320 pF*
C_1, C_2	*26 μF*
Switching frequency	*200 kHz*
Input current per cell, I_{IN}	*2.5 A*
Transistors T_1, T_2, *open drain-source resistance*	*IPW65R080CFD, 80 mOhm*
Diodes D_1,D_2, *forward voltage drop*	*C3D02060E, 1.5 V*

In the previous section, it was demonstrated that there are some optimal values of inductance and ratio between the duty cycles D_{S1} and D_{S2} for the CCM operation in all working points of the PV curve. It should be mentioned that double boost range is considered. It means that input voltage is in a range from *325 V* to *650 V*. At the same time, the input voltage in a range from *650 V* to *800 V* is acceptable and corresponds to the buck mode of the output inverter.

Fig. 7 illustrates a simplified control strategy for the proposed converter. It shows how the duty cycles depend on the input voltage. It can be seen, that the curves combine linear and nonlinear realms. Such a strategy provides a condition close to the CCM in the full operation range.

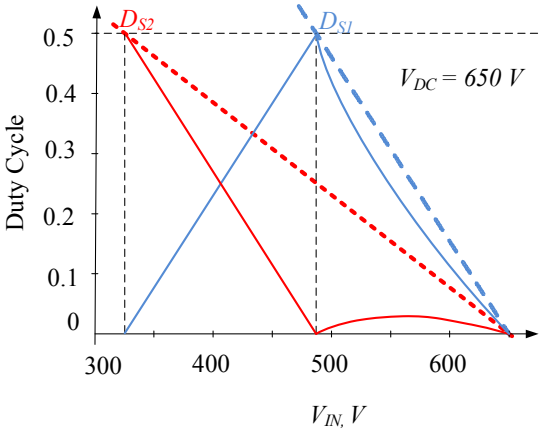

Fig. 7. Control strategy of the 3L boost dc-dc converter.

Several working points were tested. Fig. 8 illustrates simulation results of the operation point where the maximum D_{S1} duty cycle is required (D_{S1}=*0.5*).

Fig. 8*a* shows the input voltage V_{IN} and the inductor current I_{L1} and the output voltage V_{DC}. It confirms the BCM mode in the inductor current I_{L1}. The input voltage V_{IN} was about *485 V*, the input power about *1200 W*.

Fig. 8*b* shows the voltage and current waveforms across the transistor T_1 while Fig. 8*c* shows similar diagrams for the diode D_1. The main conclusion is that full ZVS was achieved.

Fig. 9 illustrates similar simulation results of the operation point where the maximum boost is required. It is possible only with D_{S2}≈*0.4*. This value is lower than that theoretically expected due the DCM.

It can be seen that some oscillations happen in the semiconductors but the ZVS is still confirmed. The input voltage V_{IN} was about *325 V* (Fig. 9*a*), the input power about *850 W*. Also, it can be seen that this point corresponds to the DCM but the output voltage corresponds to the required *650 V*, which is due to the closed loop control system.

The most interesting results are illustrated in Fig. 10. The input voltage was *550 V* at combined regulation. It means that both active states were applied D_{S1} = *0.4* and D_{S2}=*0.1*.

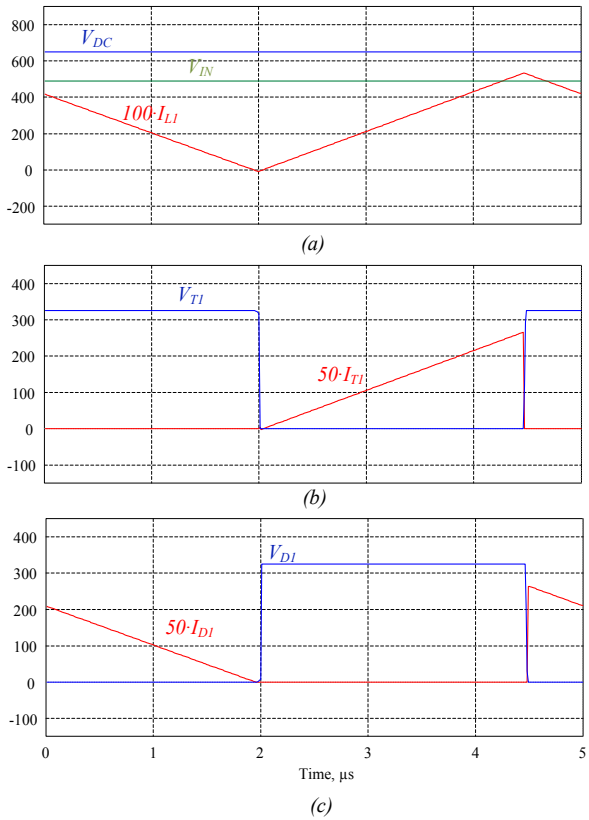

Fig. 8. Simulation results for V_{IN}=485 V, *(D_{S1}=0.5, D_{S2}=0)*: input voltage, inductor current and output dc-link voltage (a), transistor current and voltage (b), diode current and voltage (c).

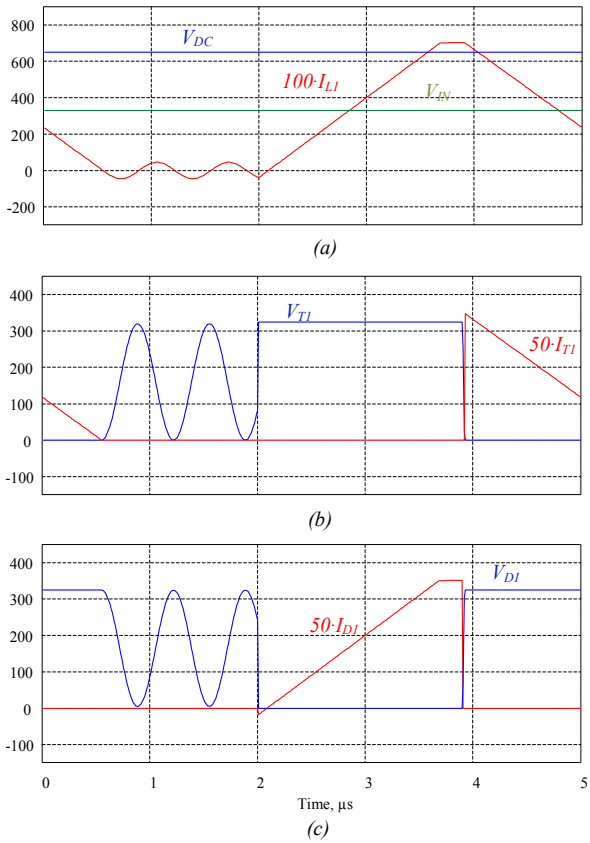

Fig. 9. Simulation results for V_{IN}=325 V, *(D_{S2}=0.4, D_{S1}=0)*: input voltage, inductor current and output dc-link voltage (a), transistor current and voltage (b), diode current and voltage (c).

Finally, it can be seen that the slope of the inductor current I_{L1} has different values and therefore the BCM is achieved without any additional oscillations. As a result, the ZVS is confirmed as well.

The waveforms discussed above demonstrates that the proposed converter is capable of operating in the ZVS in the full range of input voltage. In PV applications it is important in the partly shadowed mode or at high PV panel temperature. At low solar irradiation, instead of voltage, the output current will be smaller. It is evident that in some points, instead of the BCM, the DCM will appear, but as it was demonstrated, the ZVS approach will be valid.

The main drawback of the proposed solution lies in the discontinuous input current that requires additional decoupled capacitors in PV applications.

At the same time, it is evident that a MC structure with phase-shifted control can provide the input current CCM without decoupled capacitors. Fig. 11 shows the simulation results of the interleaved operation of the two cells.

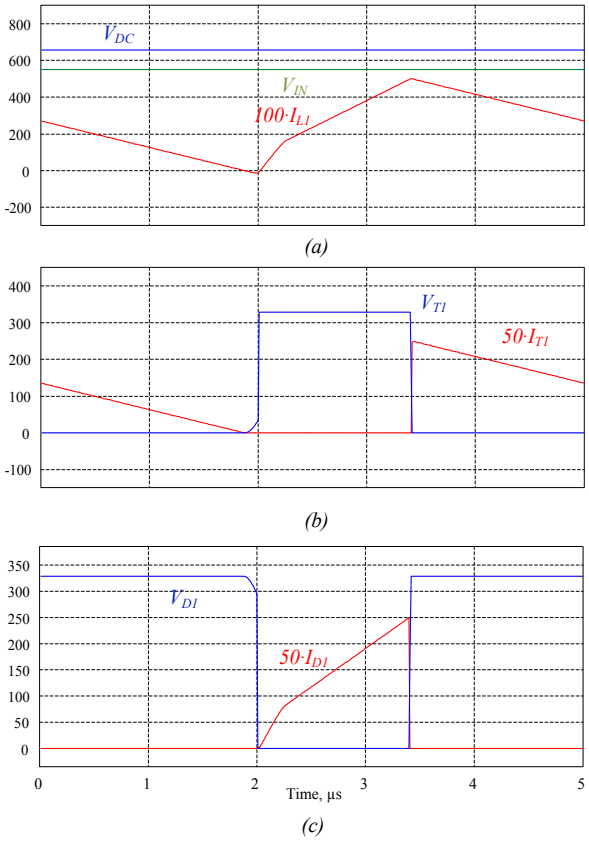

Fig. 10. Simulation results for V_{IN}=550 V, *(D_{S2}=0.1, D_{S1}=0.4)*: input voltage, inductors current and output dc-link voltage (a), transistor current and voltage (b), diode current and voltage (c).

It can be seen that the current of a separate cell has the DCM while the overall input current has non-significant input current ripple. It should also be noted that there are several control strategies that can be applied as well [13]. At the same time, current sharing between parallel cells leads to the conduction losses decreasing. Finally, Fig. 12 demonstrates the distribution of the losses in several operation points. The parameters of the semiconductors correspond to Table II and are restricted in the thermal module of PSIM, in particular, where maximum boost is required for a single cell (left column) and for two cells (middle column). Finally, the case when an average input voltage is applied is shown on the right column.

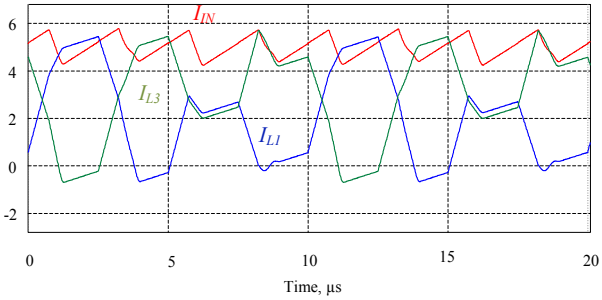

Fig. 11. Simulation results of input and inductor current for *V_{IN}=325 V, (D_{S2}=0.5, D_{S1}=0)* with two cells.

It can be seen that the conduction losses of the diodes are the main source of the overall losses of the converter. Also, should be noted that according to the simulation results, overall losses remain approximately at the same level and an overall efficiency of 99% is expected. The core losses in the inductors and wire conduction losses were not taken into account. But the main aim of the proposed idea lies not only in the overall efficiency improvement but firstly in the elimination of the switching losses.

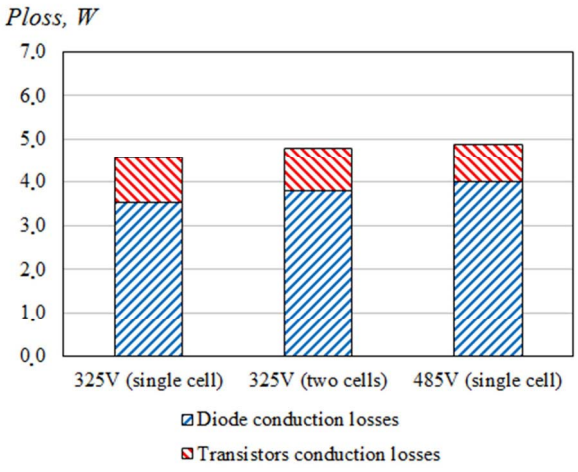

Fig. 12. Losses distribution of the 3L boost dc-dc converter.

V. CONCLUSIONS

This paper describes the full ZVS 3L boost dc-dc converter. BCM along with snubber capacitors provide ZVS operation in the whole range of operation.

The main idea lies in the combined boost regulation. It means that both active states can be applied within one switching cycle.

Analytical estimation and simulation results proved the proposed idea. In advance, it was demonstrated that the MC structure along with the interleaved control technique provide high efficiency performance and continuous

input current that makes it a promising solution for PV applications. Moreover, such an approach does not require additional current sensors or zero crossing detection.

At the same time, the performance of the algorithm can be improved by means of more complex boost regulation. More sophisticated controllers, such as neural networks or fuzzy logic, can be used for active state generation and better proximity to the BCM operation in the whole input voltage range.

ACKNOWLEDGEMENT

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